### Introduction

## Results and Discussion

## References

Recently, semiconducting two-dimensional (2D) transition metal dichalcogenide (TMD) material-based field-effect transistors (FETs) were studied actively to overcome the short channel effects (SCEs), which are fundamental issues in scaling of logic transistors for the continuation of Moore's law [1,2]. In this work, complementary  $MoS<sub>2</sub>$  and  $WSe<sub>2</sub>$  FETs were fabricated by selective patterning with alignment technique. WSe $_2$  and MoS $_2$  channels were placed on highly doped-Si/SiO $_2$  substrate using mechanical exfoliation and dry transfer method to utilize p- and n-type channel, respectively. Then, we successfully obtained ambipolar transfer curves from the complementary MoS<sub>2</sub> and WSe<sub>2</sub> FETs. In addition, I<sub>d</sub>-V<sub>d</sub> and I<sub>d</sub>-V<sub>g</sub> characteristics of each polarity transistor were analyzed to verify the ambipolar operation and several advantages of the complementary FETs. This work can provide useful information of structure design to investigate **proper electrical operation of 2D material-based ambipolar transistors.**

*Jimin Park, Jangyup Son, Sang Kyu Park, Dae-Young Jeon \**

**Institute of Advanced Composite Materials, Korea Institute of Science and Technology, Joellabuk-do 55324, South Korea**

> •**[1] Hoefflinger, B. IRDS: International Roadmap for Devices and Systems, Rebooting Computing, s3s. Nano-Chips 2030; Springer, 2020; pp 9– 17.**

> •**[2] Wang, Q. H.; Kalantar-Zadeh, K.; Kis, A.; Coleman, J. N.; Strano, M. S. Electronics and Optoelectronics of Two-dimensional Transition Metal Dichalcogenides. Nat. Nanotechnol. 2012, 7, 699– 712.**

> •**[3] W.-M. Kang, et al, "High-gain complementary metal-oxide-semiconductor inverter based on multi-layer WSe2 field effect transistors without doping", Semicond. Sci. Technol. 31 (2016).**

## Conclusions

## Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) (grant no. NRF-2017M3A7B4049167 and grant no. MSIT-CPS21081-100) and the Korea Institute of Science and Technology (KIST), Open Research Program.

**Figure 2**. Atomic force microscope (AFM) step heights of each channel layers. thickness of (a)  $WSe_2$  and (b)  $MoS_2$  layers were 26 nm and 12 nm, respectively.

**Figure 1**. Illustrations and corresponding optical microscope images showing the fabrication procedure of CFET in this work, (a)  $MoS<sub>2</sub>$  dry exfoliation and (b) WSe<sub>2</sub> dry transfer using the PDMS on the P++  $Si/SiO<sub>2</sub>$  substrate. (c) First photolithography, (d) thermal evaporation and lift-off for 10/70 nm Ni/Au electrode patterning. (e) secondary photolithography, (f) thermal evaporation and lift off for 70 nm Au electrode patterning.

20  $\begin{array}{ccc} \text{20} \end{array}$ 

In conclusion, both  $MoS<sub>2</sub>$  and  $WSe<sub>2</sub>$ -based ambipolar transistor was fabricated by mechanical exfoliation, dry transfer method, selective patterning process on single substrate. Ni and Au electrodes were contacted to multi-layers  $\mathrm{MoS}_{2}$  and  $\mathrm{WSe}_{2}$  for n- and p-type FETs, respectively. The fabricated device has shown reasonable ambipolar characteristics with ohmic-like contacts. Transfer curves and output characteristics were also analyzed in detail.

**Figure** 3. Transfer characteristics  $(I_d \text{ vs } V_g)$  of (a) p- and (b) n-type FETs. Gate bias range was -60 to 10 V, and  $V<sub>d</sub>$  was 1 V. Inset show the optical microscope image of each transistors.



**(d) Ni/Au deposition & lift-off**

**(b) WSe<sup>2</sup> dry transfer using PDMS**

The complementary metal oxide semiconductor (CMOS) industry is facing the SCEs issue caused by the down-scaling of logic devices. Therefore, CMOS using 2D TMD materials is studied. The polarity controlling of conventional siliconbased CMOS transistors is achieved by a heavy dose of impurity ion doping. However, 2D TMD-based complementary FET (CFET) can be fabricated by the difference between the work function of the contact electrode and the band gap of the semiconducting material [3].

#### **(f) Au deposition & lift-off**

**Figure 4.** (a) Ambipolar characteristics of CFET. Under the -23 V gate bias  $(V_g)$ , it depends on (b) p-type operation, over the -23 V gate bias  $(V_g)$ , it depends on (c) n-type operation. Inset show the schematics of connected circuit.



# **Ambipolar characteristics based on complementary MoS<sup>2</sup> and WSe<sup>2</sup> field-effect transistor**



30





**(c) 1st Photolithography by selective patterning**



#### **(e) 2nd Photolithography by selective patterning**





**Figure 5.** Output characteristics  $(I_d$  vs  $V_d$ ) of (a) p- and (b) n-type FETs as gate bias ( $V_g$ ) ranges from -60 to -40 V and from -20 to -20 V, respectively.



**(a) (b)**

